IN THE SPECIFICATION:

Please replace paragraph [0007] with the following amended paragraph:

[0007] Figures 1A through 1E are cross sectional views of a substrate 10 having multi-layered structures including a dielectric layer 12 formed over an underlying layer 14 which contains an electrically conducting feature 16. The underlying layer 14 may take the form of a doped silicon substrate or it may be a first or subsequent dielectric/insulating layer formed on a substrate. The dielectric layer 12 is formed over the underlying layer 14 in accordance with procedures known in the art, such as dielectric CVD, to form a part of the overall integrated circuit. Once deposited, the dielectric layer ~~16~~ 12 is patterned and etched to form interconnect features, such as vias, contacts and lines. Etching of the dielectric layer 12 can be accomplished using various generally known dielectric etching processes, including plasma etching. Although a dual damascene structure and a connection line are illustrated in Figures 1A-1E, other types of interconnect features are typically metallized using this technique as well.